AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A digital signal processor ~~(DSP)~~ to execute at least one dedicated operation of a dedicated system ~~(DFE-XDSL)~~, characterized in that said digital signal processor is a flexible digital signal processor and comprises ~~therefor~~:

an arithmetic logical unit ~~(ALU)~~ that comprises a plurality of inputs ~~(IN)~~ to receive input data ~~(DATA-IN)~~; and a predefined interconnected plurality of basic operators ~~(OP1, OP2, OP3, OP4, OP5, OP6, OP7)~~ coupled to said plurality of inputs (IN) for execution of a respective basic operation on said received input data ~~(DATA-IN)~~; and a plurality of control inputs ~~(IN-CTRL)~~ coupled between said predefined plurality of basic operators ~~(OP1, OP2, OP3, OP4, OP5, OP6, OP7)~~ and a program controller ~~(CTRL)~~; and

said program controller ~~(CTRL)~~ to activate via said plurality of control inputs ~~(IN-CTRL)~~, for at least one phase of a control program of said program controller ~~(CTRL)~~ and under control of an actual phase of said at least one phase, one or more basic operators ~~(OP1, OP2, OP3, OP6)~~ of said plurality of basic operators ~~(OP1, OP2, OP3, OP4, OP5, OP6, OP7)~~ and to enable thereby said one or more basic operators ~~(OP1, OP2, OP3, OP6)~~ to execute its respective basic operation and to realize therewith at least part of a dedicated operation of said dedicated system ~~(DFE-XDSL)~~; and

said arithmetic logical unit ~~(ALU)~~ further comprises a plurality of outputs ~~(OUT)~~ to receive, upon realization of each phase of said at least one phase of said control program, an output data ~~(DATA-OUT)~~ whereby said output data ~~(DATA-OUT)~~ represent a result of said execution of said at least one dedicated operation of said dedicated system ~~(DFE-XDSL)~~.

2. (currently amended): The flexible digital signal processor ~~(DSP)~~ according to claim 1, characterized in that said program controller comprises a start input to control a start of an execution of said control program and a finish output to sign a finishing of said control program and further characterized in that a phase of control program comprises a set of instructions being designed in accordance to a desired said at least one dedicated operation.

3. (currently amended): The flexible digital signal processor ~~(DSP)~~ according to claim 1, characterized in that said dedicated system is a digital front-end system ~~(DFE-XDSL)~~ of any digital subscriber line system.

4. (currently amended): The flexible digital signal processor ~~(DSP)~~ according to claim 3, characterized in that a dedicated operation of said dedicated system is anyone of an interpolation operation, a decimation operation, a biquad filter operation, a Finite Impulse Response filter operation, a complex to real operation inversion operation and a real to complex inversion operation.

5. (currently amended): A digital subscriber line system that comprises a digital front-end system ~~(DFE-XDSL)~~, characterized in that said digital front-end system ~~(DFE-XDSL)~~ comprises one or more flexible digital signal processors ~~(DSP)~~ according to claim 1.

6. (currently amended): A method to execute at least one dedicated operation of a dedicated system ~~(DFE-XDSL)~~ by a digital signal processor ~~(DSL)~~, characterized in that said method comprises:

receiving input data ~~(DATA-IN)~~ by a plurality of inputs ~~(IN)~~ coupled to a predefined plurality of interconnected basic operators ~~(OP1, OP2, OP3, OP4, OP5, OP6, OP7)~~ of an arithmetic logical unit ~~(ALU)~~ of said flexible digital signal processor ~~(DSP)~~; and for at least one phase of a control program of a program controller ~~(CTRL)~~:

activating via a plurality of control inputs ~~(IN-CTRL)~~ being coupled between said predefined plurality of basic operators ~~(OP1, OP2, OP3, OP4, OP5, OP6, OP7)~~ and said program controller ~~(CTRL)~~, under control of an actual phase of said control program, one or more basic operators ~~(OP1, OP2, OP3, OP6)~~ of said predefined plurality of basic operators ~~(OP1, OP2, OP3, OP4, OP5, OP6, OP7)~~; and

executing on said received input data ~~(DATA-IN)~~ one or more basic operations by said one or more activated basic operators of said dedicated system ~~(DFE-XDSL)~~; and

realizing each phase of said at least one phase of said control program and generating thereby an output data ~~(DATA-OUT)~~ representing a result of said execution of said at least one dedicated operation of said dedicated system ~~(DFE-XDSL)~~.